**Lesson Plan of the 3rd semester for session 2021-22**

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| **Name of the faculty:** | Ms. Anshita |
| **Designation:** | Assistant Professor |
| **Discipline:** | Computer Science and Engg. |
| **Semester:** | 3rd |
| **Subject:** | **DIGITAL ELECTRONICS (PCC-CSE-205G)** |
| **Lesson Plan duration:** | 15 weeks  |
| **Work Load per week in hours:** | Lectures- 03 |

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| **Week** | **Lecture****day** | **Topic** |
| 1 | 1 | Digital signals, digital circuits, AND, OR,NOT, NAND, NOR |
| 2 | Exclusive-OR operations, Boolean algebra, examples of IC gates.  |
| 3 | Number systems-binary, signed binary |
| 2 | 4 | octal hexadecimal number, binary arithmetic |
| 5 | one’s and two’s complements arithmetic, |
| 6 | codes, error detecting and correcting codes |
| 3 | 7 | Standard representation for logic functions |
| 8 | K-map representation, and simplification of logic functions using K-map |
| 9 | Minimization of logical functions. Don’t care conditions, Multiplexer |
| 4 | 10 | De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic |
| 11 | carry look ahead adder, serial adder, ALU, |
| 12 | Elementary ALU design, popular MSI chips |
| 5 | 13 | digital comparator, parity checker/generator |
| 14 | Code converters, priority encoders, decoders/drivers for display devices |
| 15 | Q-M method of function realization. |
| 6 | 16 | A1-bitmemory,thecircuitpropertiesofBistablelatch |
| 17 | The clocked SR flip flop, J-K-T and D types flip flops |
| 18 | Applications of flip flops, shift registers, applications of shift registers |
| 7 | 19 | Serial to parallel converter, parallel to serial converter, |
| 20 | Ring counter, sequence generator, ripple (Asynchronous)counters |
| 21 | Synchronous counters, counters design using flip flops |
| 8 | 22 | Special counter IC’s, asynchronous sequential counters, |
| 23 | applications of counters |
| 24 | Digital to analog converters: weighted resistor/converter |
| 9 | 25 | R-2RLadderD/A converter |
| 26 | Specifications for D/A converters, examples of D/A converter lCs |
| 27 | Sample and hold circuit, Analog to digital converters: quantization and encoding |
| 10 | 28 | parallel comparator A/D converter, dual slope A/D converter, |
| 29 | Successive approximation A/D converter, counting A/D converter |
| 30 | Memory organization and operation, expanding memory size |
| 11 | 31 | Classification and characteristics of memories, sequential memory, read only memory (ROM) |
| 32 | read and write memory(RAM), content addressable memory (CAM) |
| 33 | ROM as a PLD, Programmable logic array, Programmable array logic |
| 12 | 34 | ,complex Programmable logic devices (CPLDS), Field Programmable Gate Array(FPGA) |
| 35 | Assignment |
| 36 | Revision of unit 1. |
| 13 | 37 | Test of unit 1 |
| 38 | Assignment |
| 39 | Revision of unit 2. |
| 14 | 40 | Test of unit 2. |
| 41 | Revision of unit 3. |
| 42 | Test of unit 3. |
| 15 | 43 | Revision of unit 4. |
| 44 | Test of unit 4. |
| 45 | Problem solving. |