# Lesson Plan of the 7th semester for session 2020-21 (Jul - Dec)

**Name of the faculty:** Ms. Ayushi Chahal

**Designation:** Assistant Professor

**Discipline:** Computer Science and Engg.

**Semester:** 7th sem

**Subject:** **ADVANCED COMPUTER ARCHITECTURE**

**Subject Code:** CSE-401 F

**Lesson Plan duration:** 15 weeks

**Work Load per week in hours:** Lectures- 03, Tutorial- 01

| Week | Lecture day | Topic |
|---|---|---|
| | | **Section A** |
| 1 | 1 | **Architecture And Machines**: Some definition and terms |
| | 2 | interpretation and microprogramming |
| | 3 | The instruction set |
| 2 | 4 | Basic data types |
| | 5 | Instructions |
| | 6 | Addressing and Memory |
| 3 | 7 | Virtual to real mapping |
| | 8 | **Time, Area And Instruction Sets:** Time |
| | 9 | cost-area |
| 4 | 10 | technology state of the Art |
| | 11 | The Economics of a processor project: A study |
| | 12 | Professor Evaluation Matrix |
| 5 | 13 | Revision and Class Test of Section A |
| | | **Section B** |
| 5 | 14 | **Cache Memory Notion:** Basic Notion, Cache Organization |
| | 15 | Cache Data |
| 6 | 16 | adjusting the data for cache organization |
| | 17 | Write policies |
| | 18 | strategies for line replacement at miss time |
| 7 | 19 | Cache Environment |
| | 20 | other types of Cache |
| | 21 | Split I and D-Caches |
| 8. | 22 | On chip caches |

| | | |
|---|---|---|
| 8. | 23 | Two level Caches |
| | 24 | write assembly Cache |
| 9. | 25 | Cache references per instruction |
| | 26 | technology dependent Cache considerations |
| | 27 | virtual to real translation |
| 10. | 28 | overlapping the T cycle in V-R Translation |
| | 29 | Design summary |
| | 30 | Revision and Class Test of Section B |
| **Section C** | | |
| 11. | 31 | **Memory System Design:** The physical memory |
| | 32 | models of simple processor memory interaction |
| | 33 | processor memory modeling using queuing theory |
| 12. | 34 | open, closed and mixed-queue models |
| | 35 | waiting time, performance, and buffer size |
| | 36 | Review and selection of queuing models |
| 13. | 37 | processors with cache. |
| | 38 | Revision and Class Test of Section C |
| **Section D** | | |
| | 39 | **Concurrent Processors:** Vector Processors, Vector Memory |
| 14. | 40 | Multiple Issue Machines |
| | 41 | Comparing vector and Multiple Issue processors. |
| | 42 | **Shared Memory Multiprocessors**: Basic issues, partitioning, synchronization and coherency |
| 15. | 43 | Type of shared Memory multiprocessors |
| | 44 | Memory Coherence in shared Memory Multiprocessors. |
| | 45 | Revision and Class Test of Section D |